

BUR92000008
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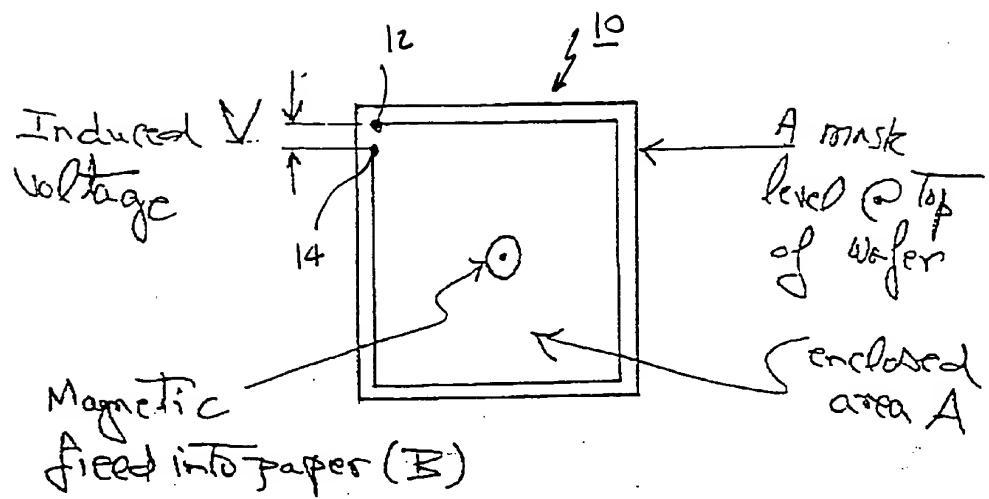


FIG.1

09612545 00019000

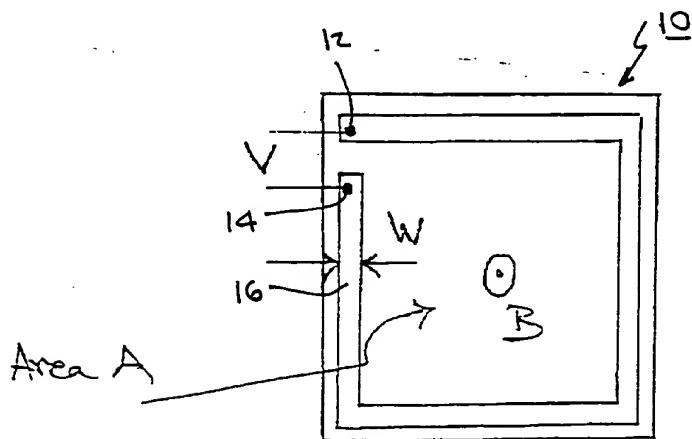
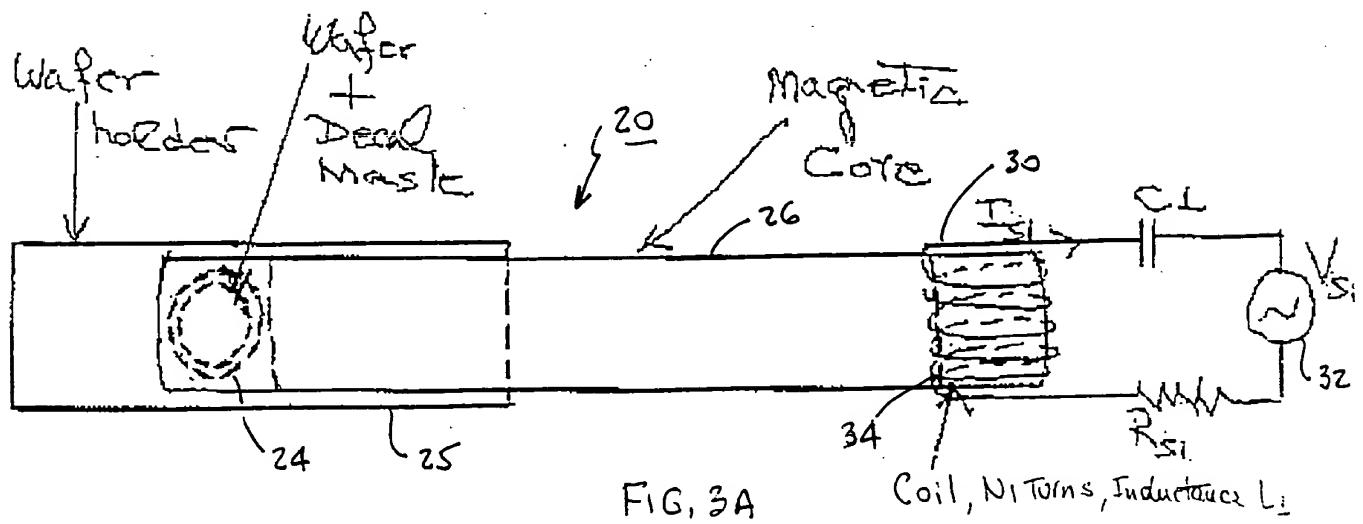
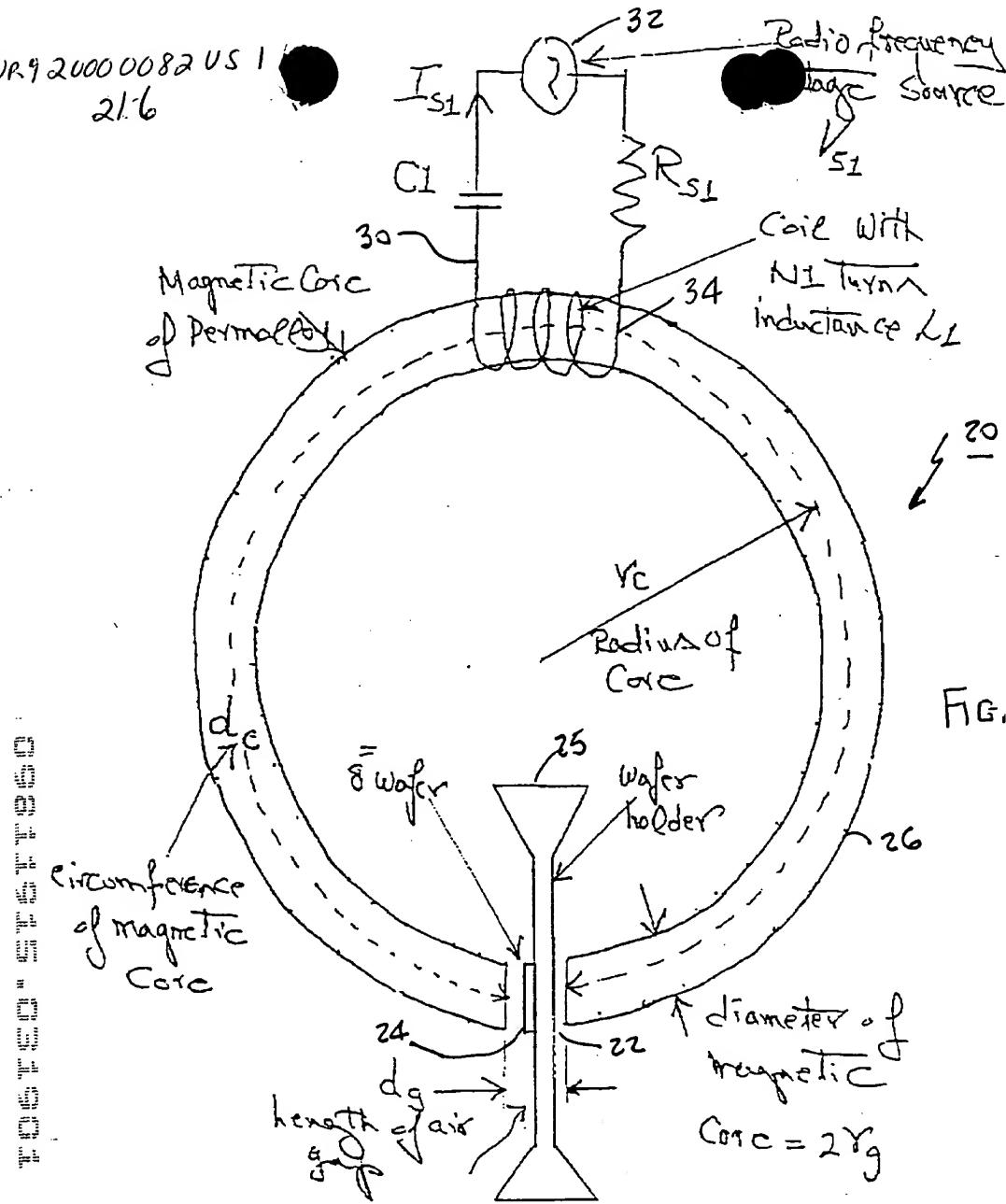


FIG.2

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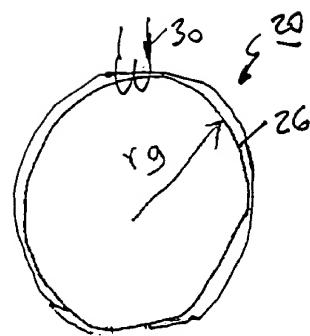


FIG. 4

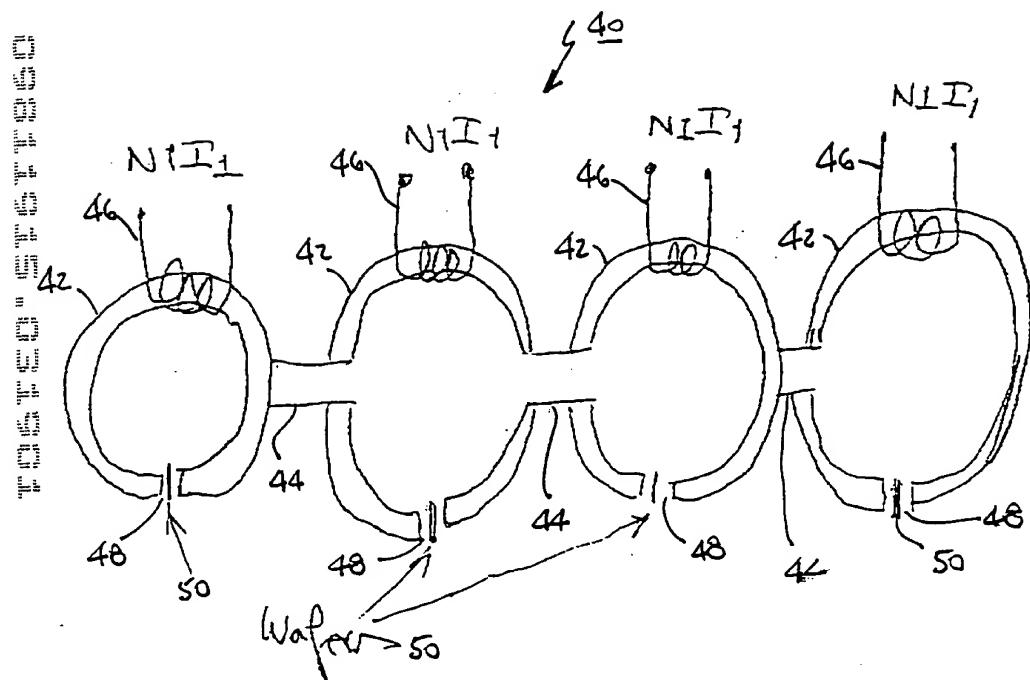


FIG. 5

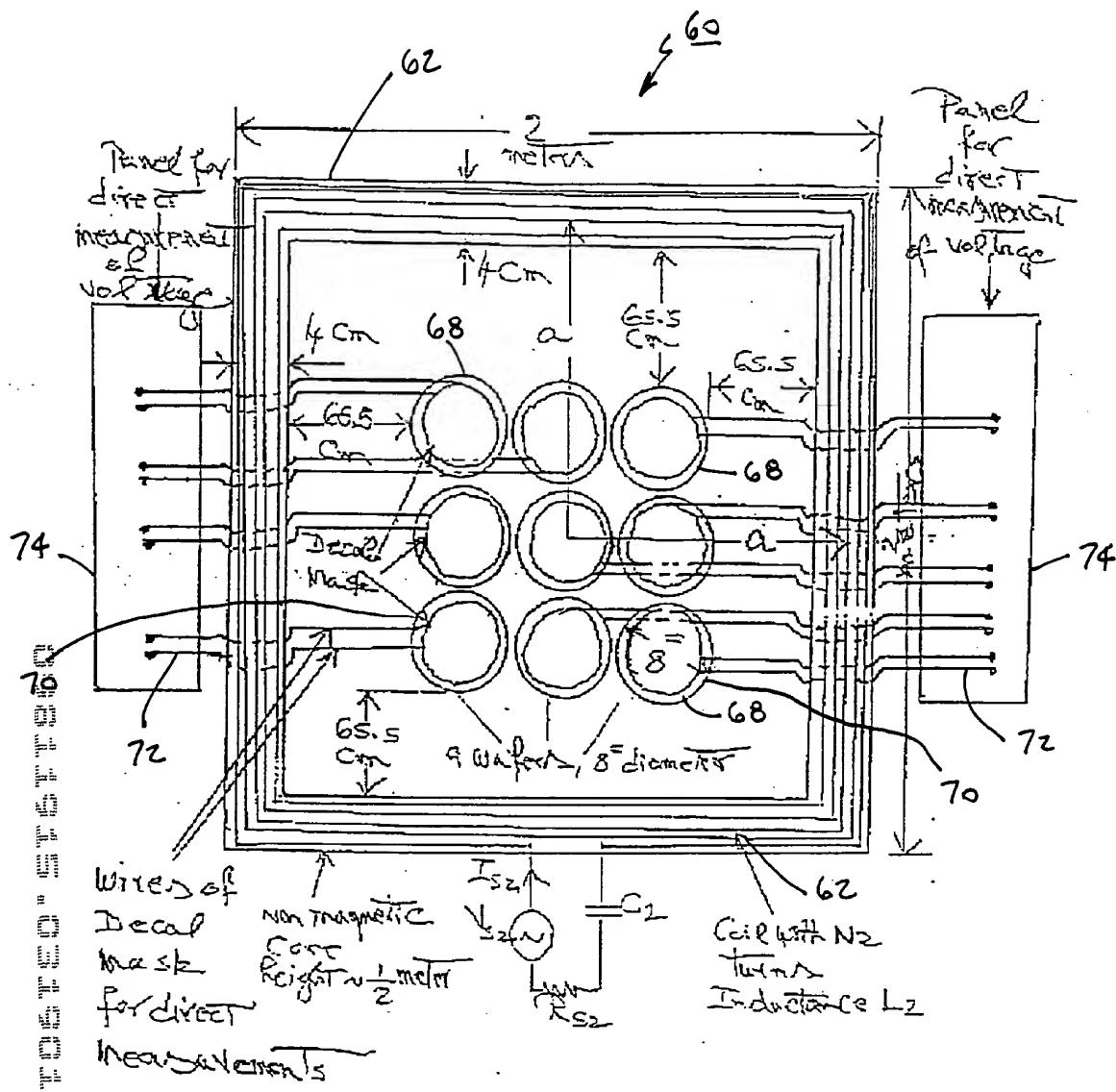


FIG. 6

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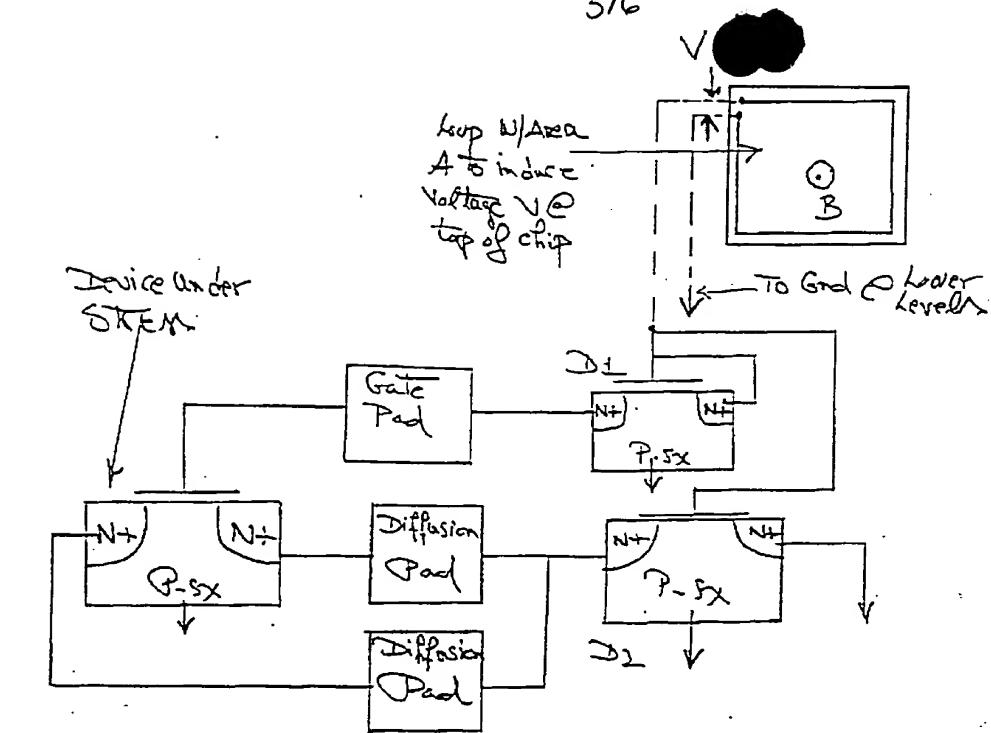


FIG. 7

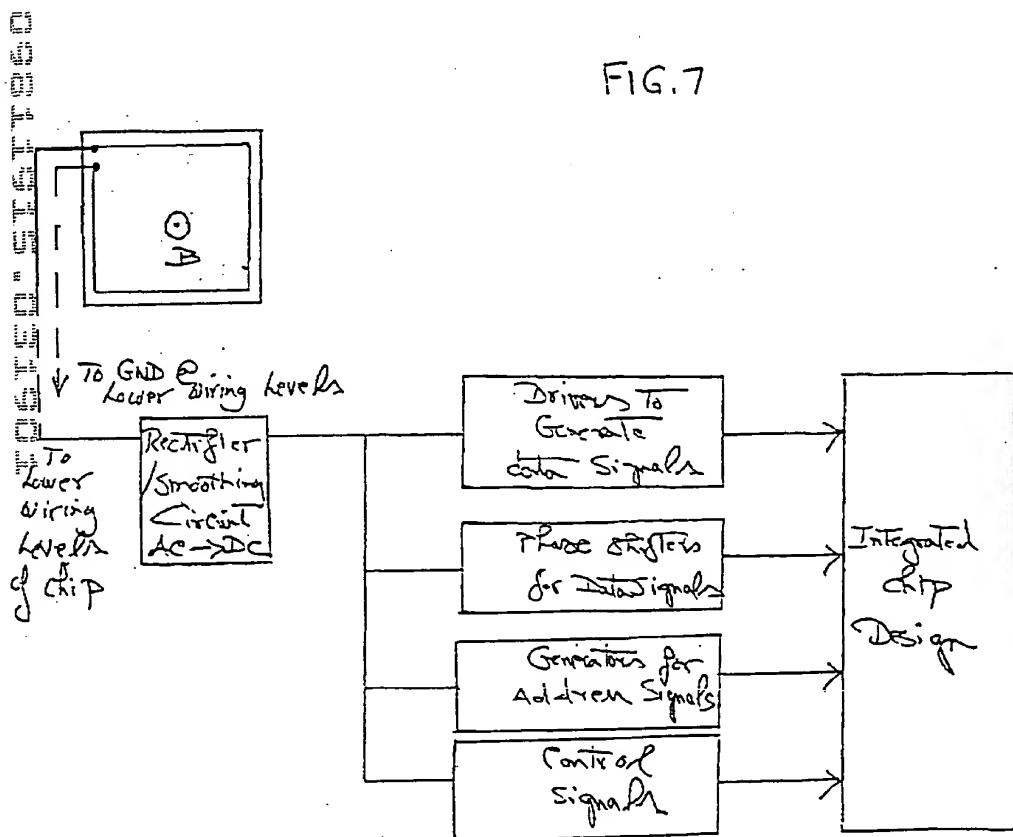
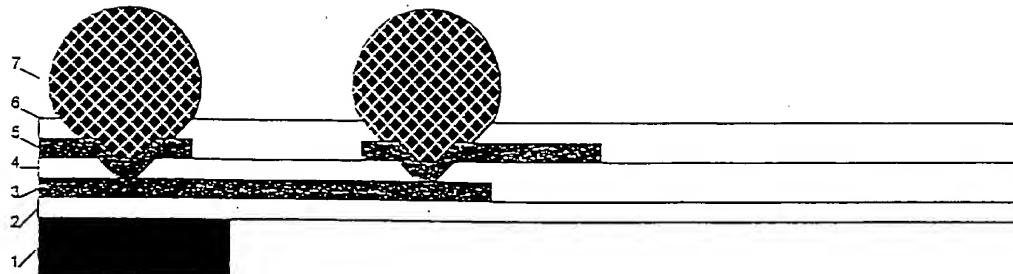
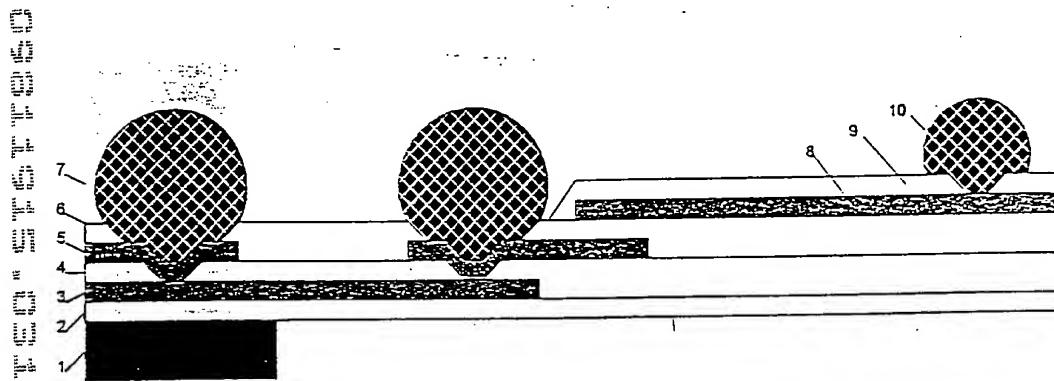


FIG. 8



Structure option 1 - appropriate for use with wafers having P- silicon substrates

FIG. 9



Structure option 2 - appropriate for use with wafers having P+ silicon substrates

Wiring layer (8) is a blanket or mesh structure that shields the active chip from the magnetic field. Wiring layer (8) is constructed in the same manner as wiring layer (3). Passivation layer (9) is constructed in the same manner as layer (4). Solder bump structure (10) is constructed in the same manner as bump (7) with adjustment to deposited volume as necessary.

FIG. 10